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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,474	06/23/2000	Joseph Herbst	108339-09036	1343

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EXAMINER	
SHAH, SAUMIL R	

ART UNIT	PAPER NUMBER
2186	7

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/602,474	HERBST, JOSEPH	
	Examiner	Art Unit	
	Saumil Shah	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/23/2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

The word "poolis" (note page 5, line 30) should be replaced by the words "pool is".

The word "wshen" (note page 60, line 3) should be replaced by the word "when".

The words "data pocket" (note Figure 8, 112) should be replaced by "data packet".

A brief description of Figure 39 has not been provided in the disclosure.

Claim Objections

2. Claim 6 objected to because of the following informality:

The word "beck" (note claim 6, line 10) should be replaced by "back".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3-4, 7, 12-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. In claim 3, line 24, it is unclear what receives the released memory address in the first clock cycle. The applicant is required to correct the language of claim 3 to clarify this critical feature so that a basis to search for prior art can be established.

b. In claim 3, lines 25-26 are unclear with regard to the cycle in which the address is passed to the module requesting the address. One interpretation is that the address is passed in the very next cycle and for this interpretation, the following claim language is suggested

"....passing off the released memory address in the next clock cycle to the module requesting the next available memory address"

c. Note that claim 4 depends on claim 3. Also, claim 4 has the feature of a memory address pointer (line 29). But, it is unclear as to what this pointer is associated with. There is no suggestion of the context of this pointer in claims 3 and 4.

d. In claim 7, the method comprises that of claim 6 and further comprises passing off the address released without incrementing or decrementing the address pointer.

However, claim 6 mentions "passing off an address released back to the stack" (note line 9). But an address can be said to be in a stack only if the pointer

is incremented or decremented as is well known in the art. This contradiction makes the claim unclear.

e. In claim 12, the apparatus has the features of claim 11 and is further configured to read said available memory address and write said released memory address in the same clock cycle without adjusting said address pointer. However, an address is said to be in a memory pool only if the address pointer is incremented or decremented as is well known in the art. This contradiction with the features of claim 11 makes the claim unclear.

f. In claim 13, it is unclear what requests an available memory address and releases a memory address (lines 14-16). The applicant is required to correct the language of claim 3 to clarify this critical feature so that a basis to search for prior art can be established. Note, claims 14-19 depend on claim 13.

g. In claim 20, it is unclear what requests an available memory address and releases a memory address (lines 15-17).

h. In claim 20, it is also unclear when the address is passed off (lines 16-17).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 5, 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Heddes et al (US Patent No. 5,432,908).

a. With regard to claim 1, Heddes et al disclose a method for managing memory in a network switch (note column 3, lines 20-23), said method comprising the steps of:

providing a memory, wherein he memory includes a plurality of memory locations configured to store data therein (note column 3, lines 24-26);

providing a memory address pool having a plurality of available memory addresses arranged therein, wherein each of the plurality of memory addresses corresponds to a specific memory location (note column 4, lines 22-28 where the "free buffer linked list" teaches a memory address pool);

providing a memory address pointer, wherein the memory address pointer indicates a next available memory address in the memory address pool (note column 4, lines 28-30 where the "BCR" contains a pointer to the next "BCR" which is free);

reading available memory addresses from the memory address pool using a last in first out operation (note column 8, lines 39-45 where the free buffer is popped from the stack and it is well known in the art that a stack operates in a last-in first-out manner as can also be seen from column 8, lines 42-48);

writing released memory addresses into the memory address pool (note column 8, lines 46-48); and

adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool (note column 8, lines 39-45 and also it is well known in the art that a stack increments/decrements a pointer when an element is added/subtracted from it).

b. With regard to claim 2, Heddes et al disclose the method for managing memory in a network switch as recited in claim 1, wherein the steps of reading available memory addresses and writing released memory addresses are initiated during a second clock cycle when the reading step and the writing step are requested in a first clock cycle (note column 10, lines 36-54 where it is clear that the request/release process is initiated from the cycle after receiving the request/release).

c. With regard to claim 5, Heddes et al disclose a method of managing memory, said method comprising the steps of:

providing a memory having a predetermined number of memory storage locations therein (note column 3, lines 39-41 which teaches that there are an equal number of BCRs corresponding to buffers. Thus, the number of buffers or "memory storage locations" is predetermined);

providing a predetermined number of addresses in a stack, each of the predetermined number of addresses corresponding to a unique memory storage location (note column 3, lines 39-42 which teaches that there are is a BCR corresponding to each buffer); and

providing an address pointer for indicating a next available address to be used from the predetermined number of addresses in the stack (note column 4, lines 26-31), wherein the address pointer releases an address in a last-in first-out type operation (note column 4, lines 32-33 where the linked list behaves like a stack and it is well known in the art that a stack operates in a last-in first-out manner).

d. With regard to claim 8, Heddes et al teach an apparatus for managing memory in a network switch, said apparatus comprising:

a memory address pool having a plurality of memory addresses, each of said plurality of memory addresses corresponding to an individual memory location in a memory (note column 4, lines 22-28 where the "free buffer linked list" teaches a memory address pool); and

a memory controller in connection with said memory and said memory address pool (note figure 2 where buffer manager teaches a memory controller and is connected to the memory and the memory address pool (stack/ FIFO)),

wherein said controller manages an address pointer for indicating a next available memory address in said memory address pool (column 4, lines 62-64 where the stack manager is a part of the "memory controller" as is shown in figure 2).

e. With regard to claim 9, Heddes et al teach the apparatus of claim 8, wherein said memory address pool further comprises a cell free address pool

(note figure 2, where the stack is the "cell free address pool", note column 4, lines 32-33).

f. With regard to claim 10, Heddes et al teach the apparatus of claim 8, wherein said memory address pool further comprises a slot free address pool (note figure 2, where the FIFO is the "slot free address pool", note column 4, lines 37-38).

g. With regard to claim 11, Heddes et al teach the apparatus of claim 8, wherein said memory controller is further configured to read an available memory address from said memory address pool and to write a released memory address to said address pool (note column 8, lines 39-45 where the pointer is taken from the stack and also pushed onto the stack).

h. No prior art rejection could be made for claims 3-4, 7, 12-20 without overcoming the 35 USC 112 rejections as the mentioned critical features could be interpreted in many ways.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heddes et al (US Patent No. 5,432,908) in view of Hine (US Patent No. 5,652,864).

With regard to claim 6, Heddes et al teach everything of claim 5 as is mentioned above. Hine teaches a method that comprises the step of passing off an address released back to the stack (note column 8, lines 12-14 where the address is returned and the use of the stack has already been taught by Heddes et al) to a request for an available address when a release of an address back to the stack occurs in the same clock cycle as the request for an available address (note column 1, lines 26-28 which teaches block release and allocation concurrently).

Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have added Hine's feature of passing an address released back to the stack to a request for an available address when the request and release occurs in the same cycle in the Heddes et al. system, since this would allow parallelism in release/granting of addresses amongst various processes/entities and thus make the memory management faster.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saumil Shah whose telephone number is 703-305-8786. The examiner can normally be reached on 9:00 AM to 5:30 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Saumil Shah
Patent Examiner
Art Unit 2186

14 November, 2003

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER